

FIG.1

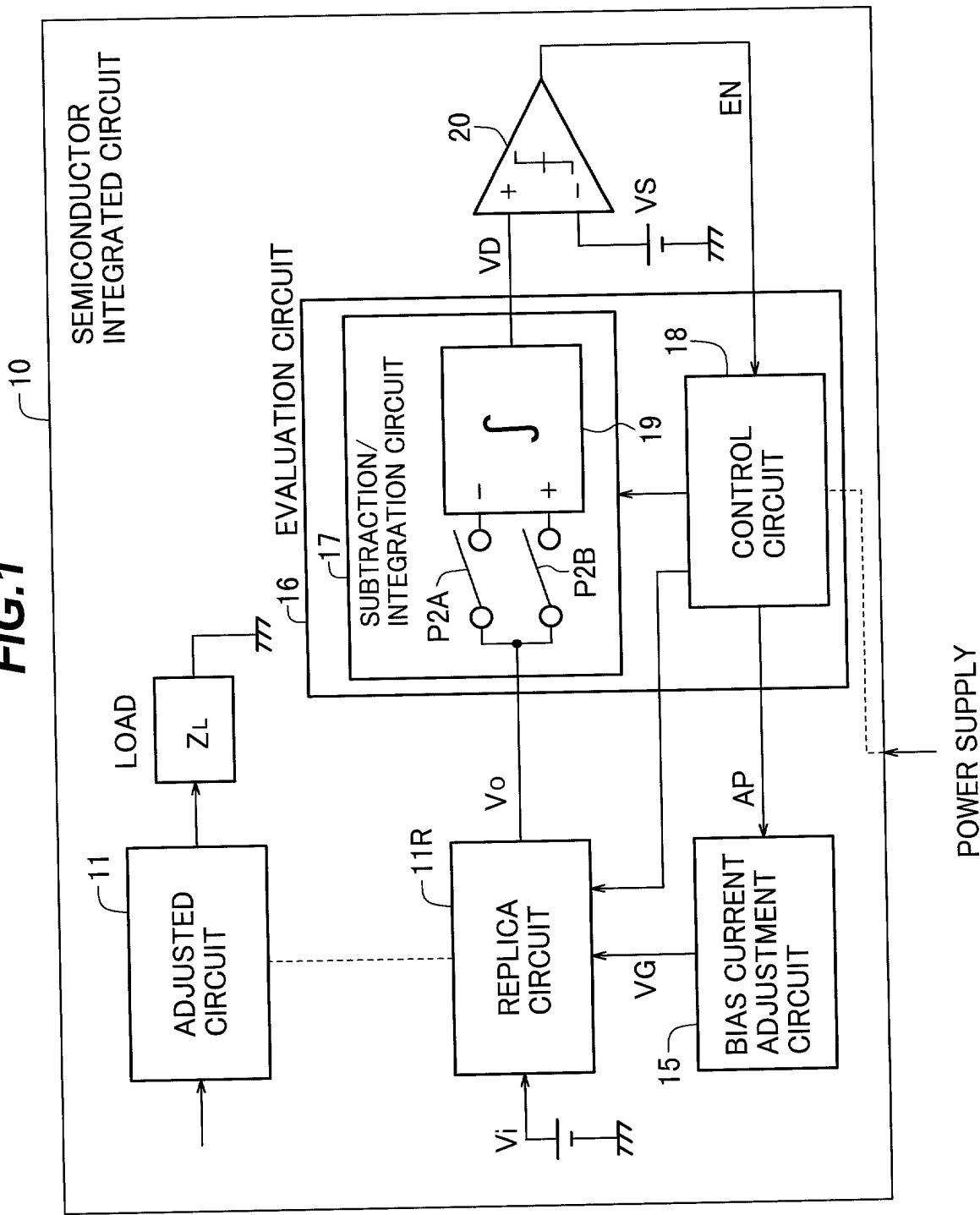


FIG.2

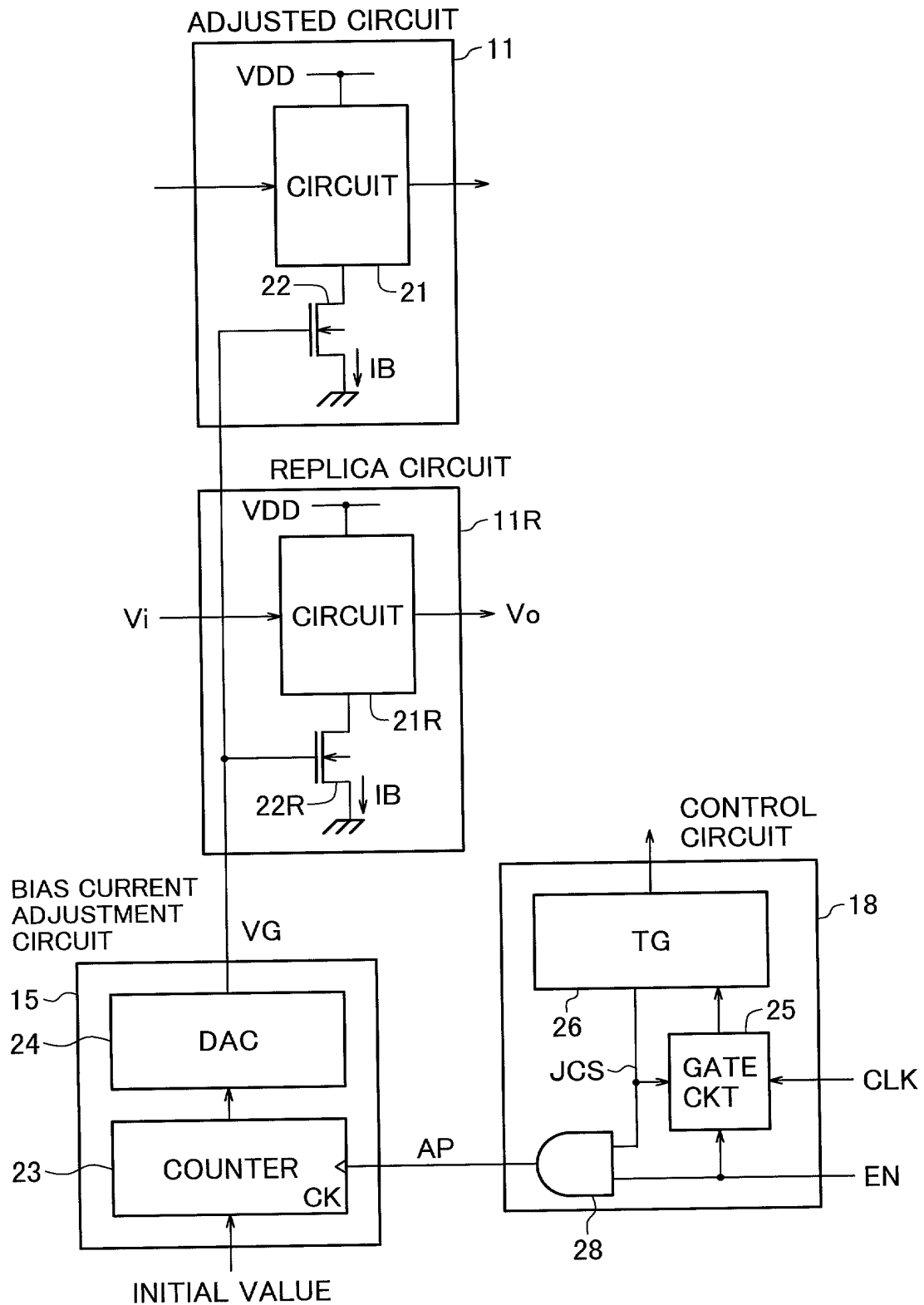


FIG.3

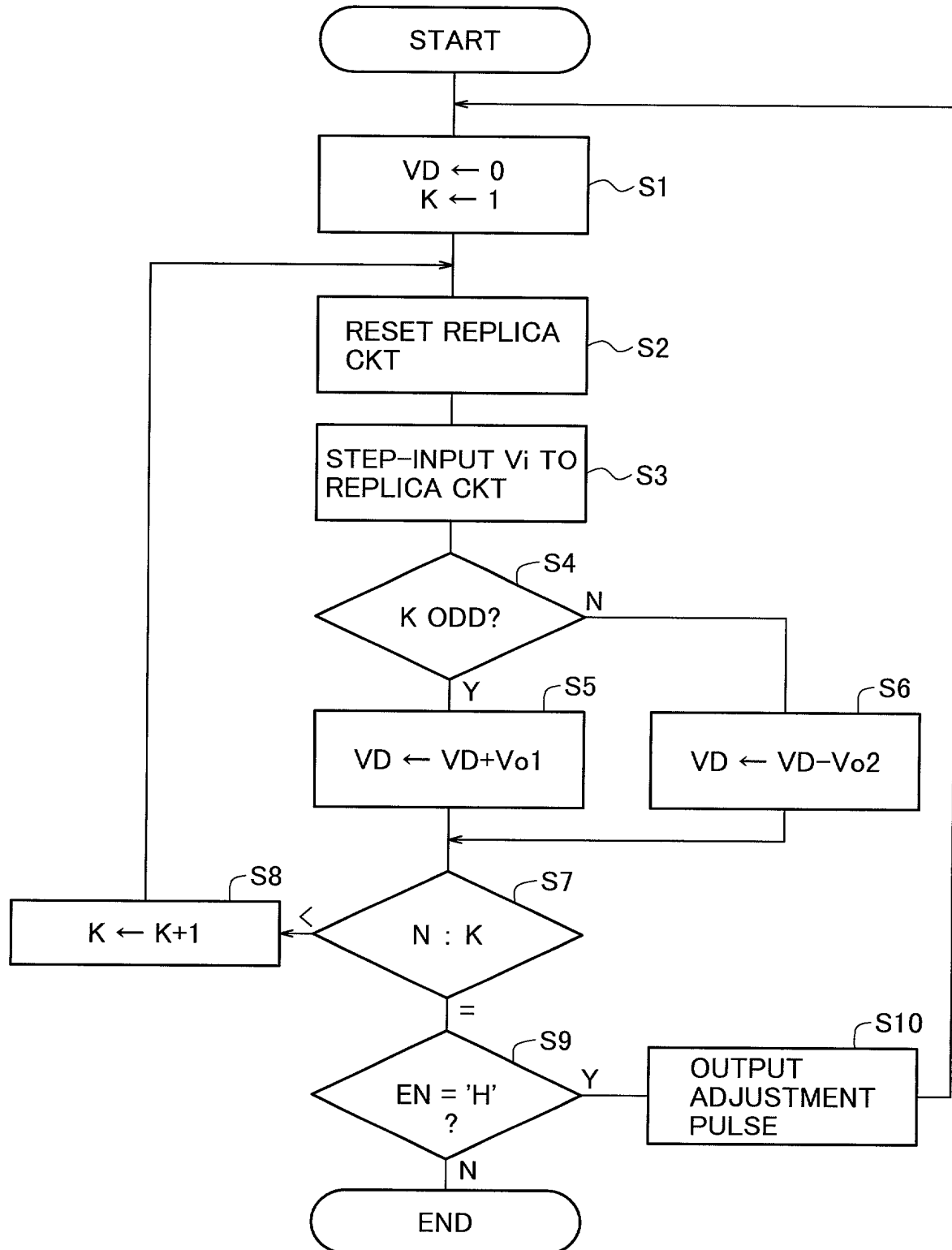


FIG.4(A)

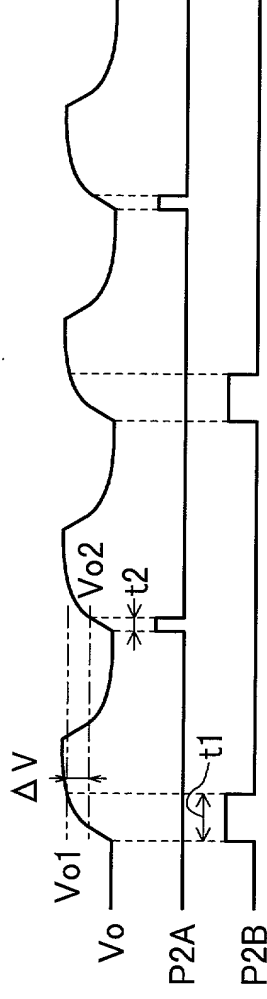


FIG.4(B)

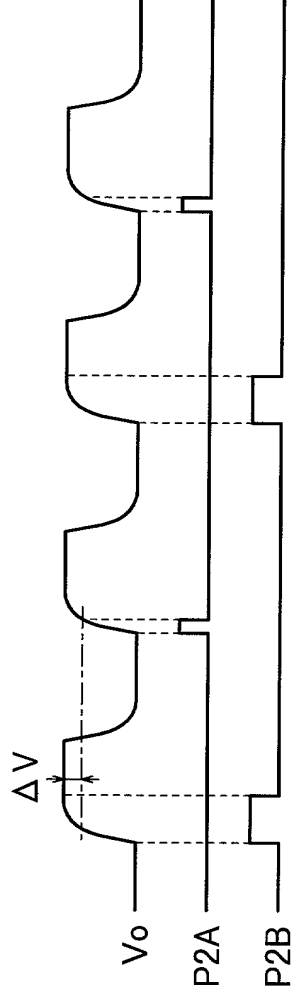


FIG.4(C)

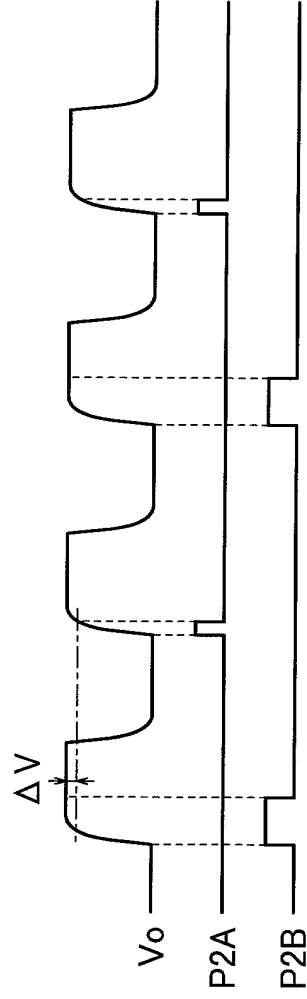


FIG.5(A)

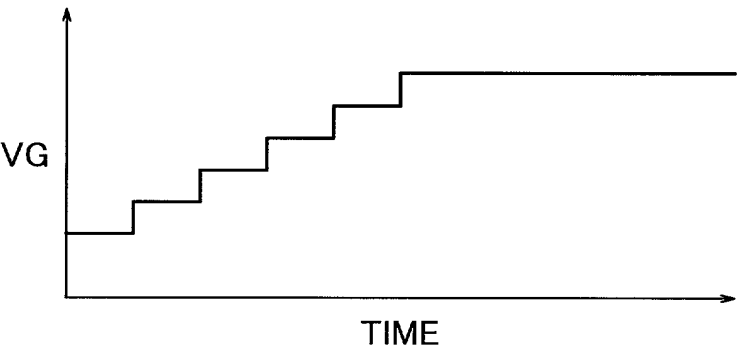


FIG.5(B)

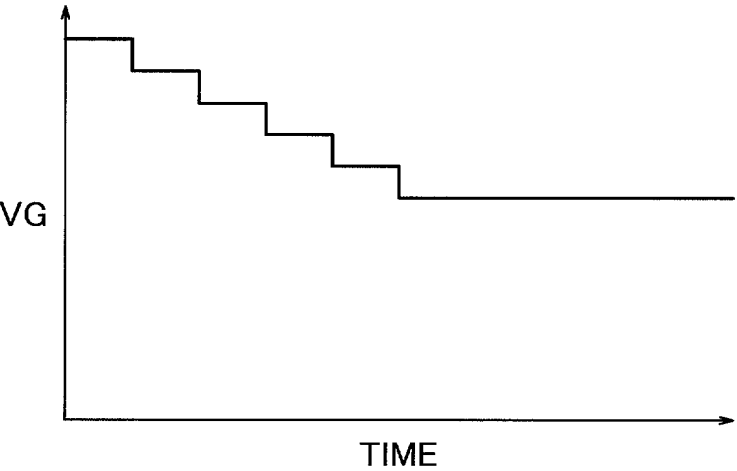


FIG.5(C)

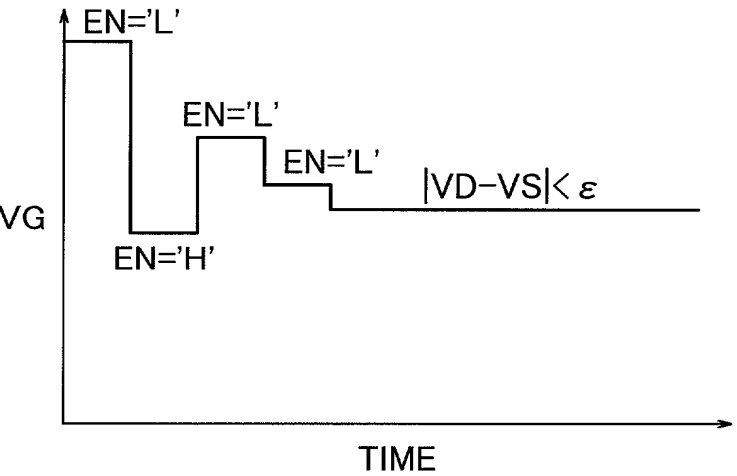




FIG. 7

SUBTRACTION/INTEGRATION CIRCUIT

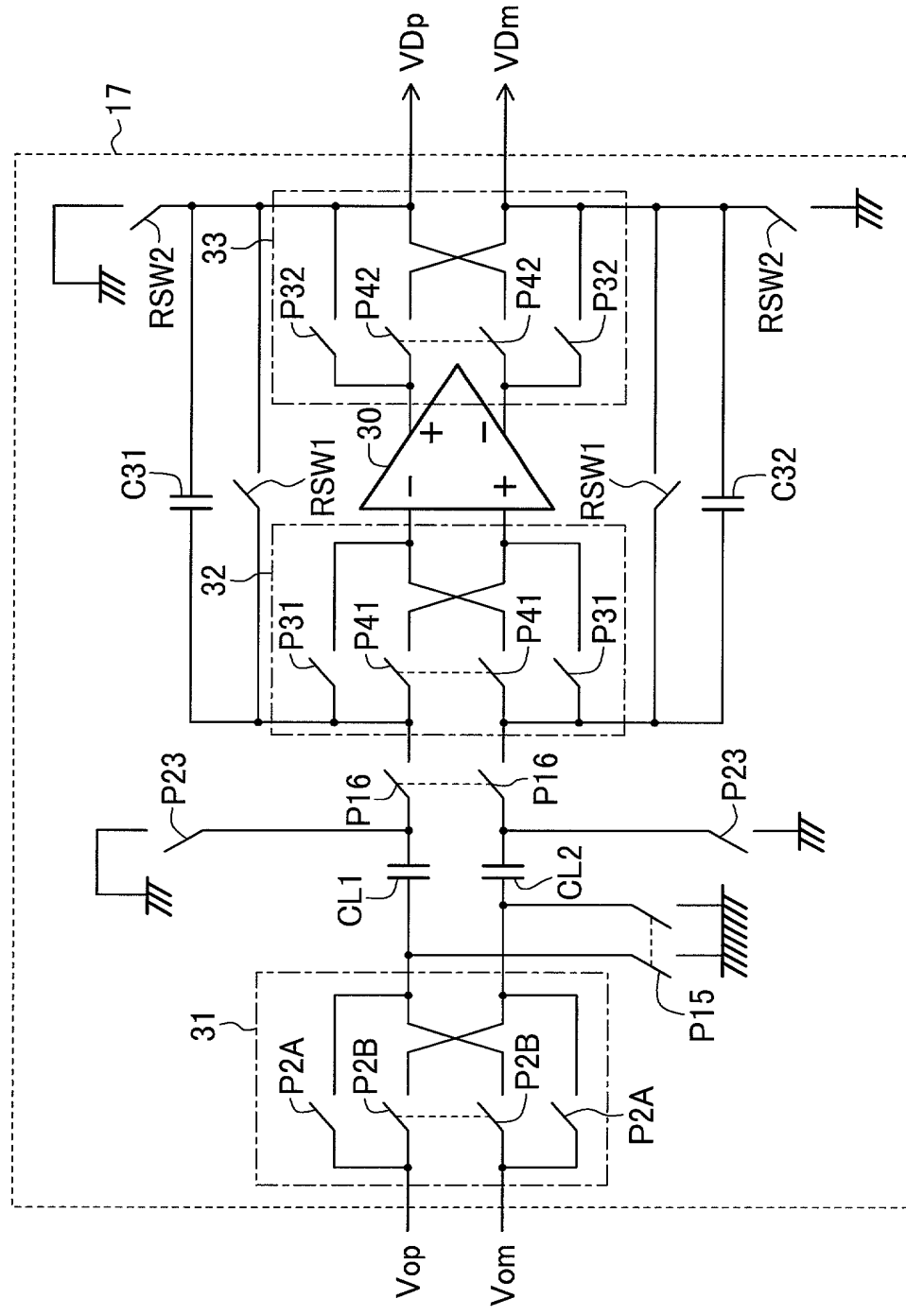


FIG. 8

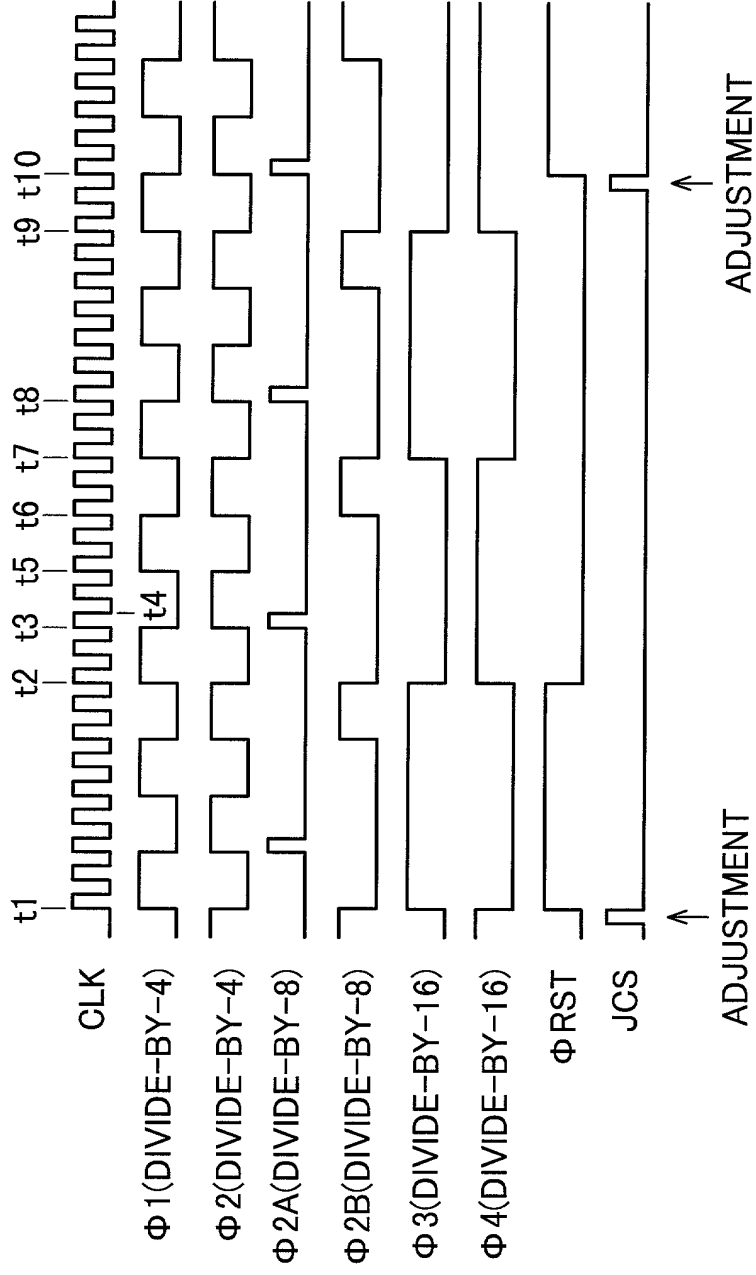


FIG.9
prior art

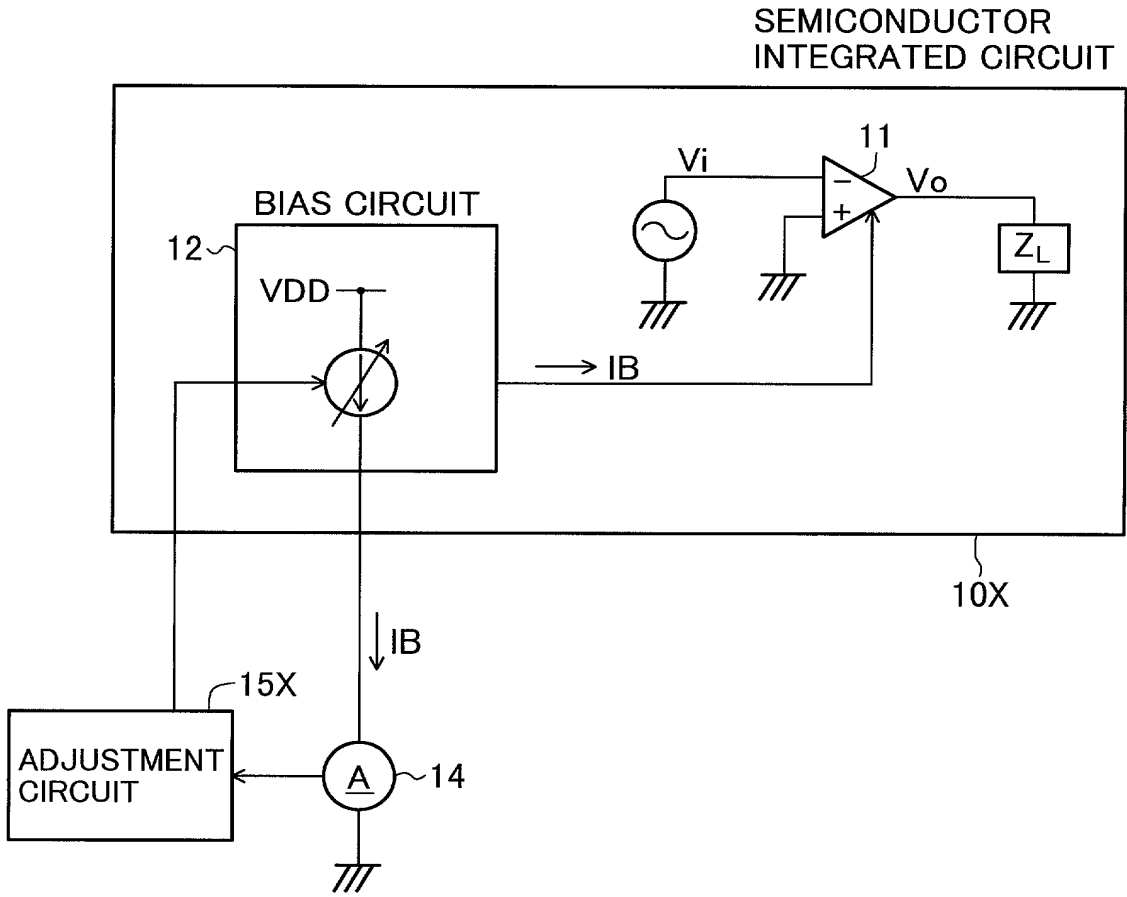


FIG.10
prior art

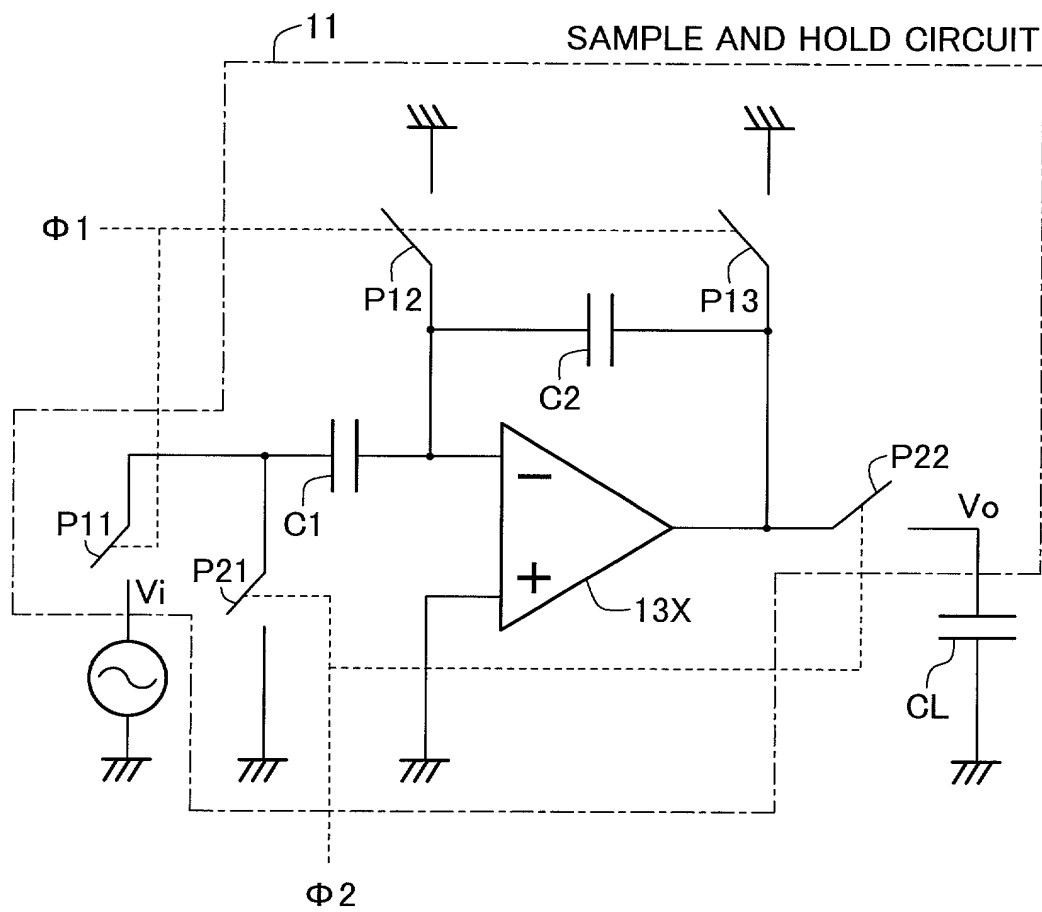


FIG.11
prior art

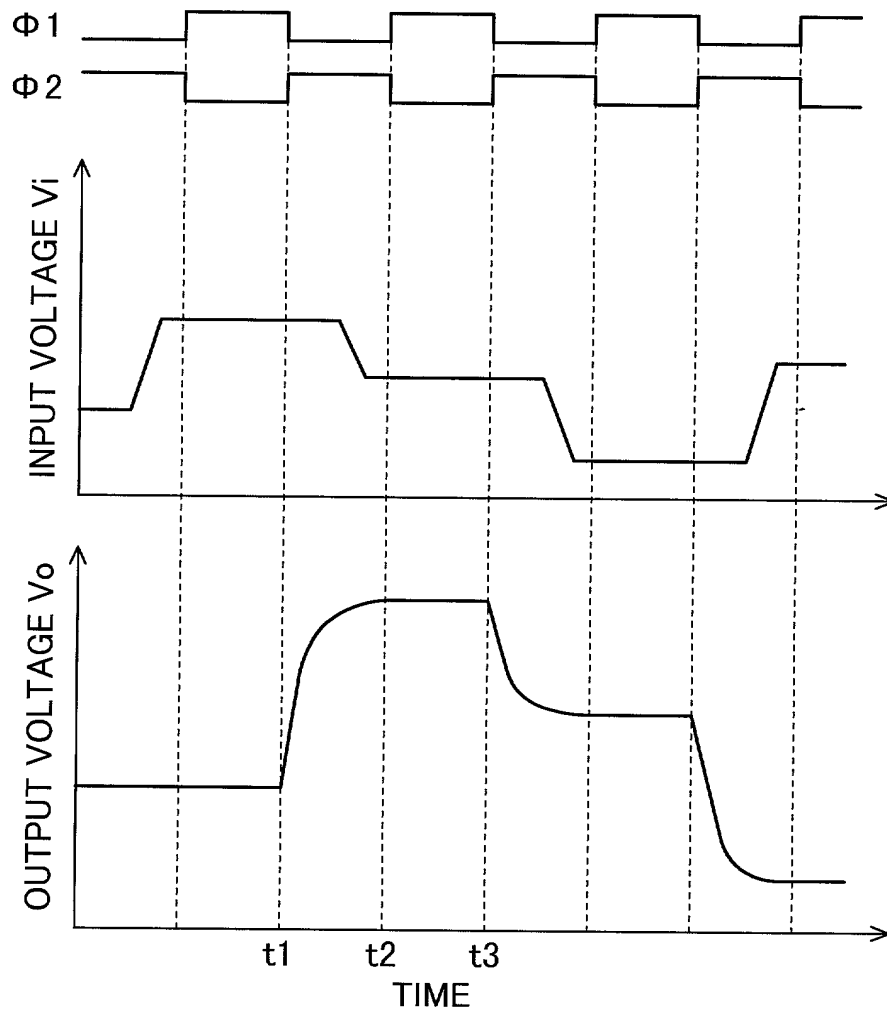


FIG.12
prior art

